In the Claims

Please replace all prior versions, and listings, of claims in the application with the following list of claims:

1. (Previously presented) A method for compensating for temperature effects during operation of a semiconductor circuit comprising:

scaling an output value of said circuit to a desired output value at a first temperature; and

altering the temperature of the circuit from the first temperature to a second temperature and correcting said output value at the second temperature to match said desired output value, such that the correction which is to provide said desired output value at the second temperature does not change the output value at the first temperature, matching being effected by the addition or subtraction of the difference between two balanced trimming PTAT and CTAT currents.

2. (Original) The method of claim 1 wherein the step of scaling said output value is effected by the addition or subtraction of a constant voltage value.

3. (Original) The method of claim 2 wherein said constant voltage value is generated by forcing a constant current through a resistor of said circuit.

4. (Original) The method of claim 3 comprising generating said current from a balanced combined PTAT and CTAT current.

5. (Original) The method of claim 3 comprising generating said current from reflecting a reference voltage across said resistor.

6. (Cancelled)

7. (Previously presented) The method of claim 1 wherein said trimming currents are such that at said first temperature the difference between each current is zero and the combined current value has a double slope compared to a slope value of each individual current.

8. (Previously presented) The method of claim 1, comprising, between said scaling and said matching step the additional step of tuning of said trimming currents such that the difference between said PTAT and CTAT currents at said first temperature is equal to zero.

9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)

17. (Previously presented) A semiconductor circuit adapted to provide compensation for temperature effects during operation comprising:

means for scaling an output value of said circuit to a desired output value at a first temperature; and

means for altering the temperature of the circuit from the first temperature to a second temperature and matching said output value, at the second temperature, to said desired output value, such that said desired output value at said first temperature remains unchanged, the matching being provided by the addition or subtracting of the difference between two balanced trimming PTAT and CTAT currents.

18. (Original) The circuit of claim 17 wherein the means for scaling said output comprises a multiplexor for adding or subtracting said output by a constant voltage value.

19. (Original) The circuit of claim 18 wherein the constant voltage value is generated by forcing a constant current through a resistor of said circuit.

20. (Original) The circuit of claim 19 wherein the value of the constant current is controlled by a current source coupled to a DAC, a value of a user controlled input code applied to said DAC to determine the value of the constant current.

21. (Original) The circuit of claim 20 wherein the addition or subtraction of the constant voltage value is controlled by at least one of said multiplexors coupled to two outputs of said DAC, to determine whether the constant voltage value is to be added or subtracted.

22. (Original) The circuit of claim 20 wherein the addition or subtraction of the constant voltage value is controlled by a second input to the said DAC.

23. (Cancelled)

24. (Previously presented) The circuit of claim 17 wherein said trimming currents are such that at said first temperature the difference between each current is zero and the combined current value has a double slope in the temperature domain compared to the slope of each individual trimming current.

25. (Previously presented) The circuit of claim 17 wherein the PTAT and CTAT trimming currents are controlled by a first and a second DAC, the output of said first and second DAC connected to at least one multiplexor, whereby a control signal applied to said multiplexor controls the addition or subtraction of said difference.

26. (Previously presented) The circuit of claim 17 comprising tuning means for the tuning of said trimming currents such that the difference between said PTAT and CTAT currents at said first temperature is equal to zero.

27. (Previously presented) The circuit of claim 26 wherein said tuning means comprises a tuning DAC coupled to a source of one of said currents, such that tuning may be achieved by adjusting a value of a user controlled input to said tuning DAC.

28. (Original) The circuit of claim 20 wherein the values of the user controlled inputs codes are stored in memory.

29. (Original) The circuit of claim 27 wherein the value of the user controlled input code is stored in memory.

30. (Previously presented) The circuit of claim 24 wherein the values of said trimming currents providing said difference are stored in memory.

31. (Currently amended) A semiconductor circuit adapted to provide compensation for temperature effects during operation, the circuit comprising a digital control means for:

digitally scaling an output voltage of said circuit to a desired output voltage value at a first temperature; and

digitally matching said output voltage value, at a second temperature, to said desired output voltage value, such that said desired output voltage value at said first temperature remains unchanged,

wherein a constant current is generated by a balanced combination of PTAT and CTAT current sources, each current source coupled to a DAC, the value of an input code applied to an input of each DAC determining the value of the constant current and wherein the addition or subtraction of the constant voltage value is controlled by a second input to each DAC.

32. (Cancelled)

33. (Original) The semiconductor circuit of claim 31 wherein said digital control means comprises a register, coupled to the inputs of each DAC, wherein the output values from said register determine the value of the input codes to each DAC.

34. (Original) The semiconductor circuit of claim 33 wherein said register is connected to a digital control unit and memory, the value of said input codes are stored in said memory, and the transfer of said input codes from memory to the register is controlled by said digital control unit.

35. (Cancelled)

36. (Cancelled)

37. (Cancelled)

38. (Cancelled)